# High-Voltage p-GaN HEMTs With OFF-State Blocking Capability After Gate Breakdown

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***Abstract*— In this letter, we report high-performance p-GaN HEMTs on Si with robust gate operation. For the first time, the preserved OFF-state drain blocking capability has been demonstrated in p-GaN HEMTs after forward gate breakdown. Benefitting from the reduced metal/p-GaN contact region, the gate breakdown was limited to take place only at the metal/p-GaN junction, with the p-GaN/AlGaN/GaN junction intact. The device shows state-of-the-art characteristics with a large threshold voltage of 1.75 V at $I_D$ of 100 $\mu$A/mm (2.3 V by linear extrapolation), a high maximum drain current of 610 mA/mm at $V_{GS}$ of 8 V, a low specific ON-resistance of 1.8 m$\Omega \cdot$ cm$^2$, and a high breakdown voltage of 1100 V defined at $I_D$ of 1 $\mu$A/mm with grounded substrate.**

***Index Terms*— HEMT, p-GaN gate, normally-OFF, OFF-state, gate breakdown.**

## I. Introduction

NORMALLY-OFF GaN high electron mobility transistors (HEMTs), with the merit of inherent fail-safe operation, fast switching speed, and low reverse conduction loss, have shown tremendous promise for ef cient power switching applications [1]. Several approaches, including gate recess, p-(Al)GaN gate, and uorine implantation, can be employed to realize normally-OFF GaN transistors and excellent device metrics such as high breakdown voltage ($V_{BR}$) and low ON-resistance ($R_{ON}$) have been demonstrated [2] [11]. Among the aforementioned methods, p-(Al)GaN gate technology is currently the only one being employed in commercialized normally-OFF GaN HEMTs because of better controllability and stability in threshold voltage [1], [12], [13]. However, as a result of the metal-semiconductor gate contact scheme, either Schottky or Ohmic, the gate stack of p-GaN HEMTs is quite vulnerable, typically showing large gate leakage ($I_G$) and limited gate swing [6], [7]. An excessively high forward gate bias, e.g., gate voltage spikes at high speed switching transient, would often lead to catastrophic gate breakdown, with sudden and irreversible increase of gate leakage, thus device failure. To ensure the fail-safe operation of p-GaN HEMT power switches, it is vital to maintain the OFF-state blocking capability of the p-GaN HEMTs at $V_{GS}$ of 0 V, i.e., a low standby drain leakage current, in case the gate breakdown occurs due to unexpected excessive gate overdrive. Otherwise, the surge of drain current after gate breakdown combining with a high OFF-state drain voltage can cause severe damage to the whole switching system, not only the device itself.

However, in all the reported p-GaN HEMTs, to our best knowledge, the forward hard breakdown of the gate stack increases both the forward and reverse $I_G$ by several orders of magnitude, resulting in signi cant increase of OFF-state $I_D$ and complete loss of gate control [14] [17]. The failure mechanism of forward gate breakdown of p-GaN HEMTs is still under debate [15], [16], [18]. It is found that in the conventional p-GaN HEMT design, the gate metal is commonly self-aligned with the p-GaN gate [8], [19], [20], conveniently using the gate metal as the etching mask for p-GaN patterning. This design can spread the gate potential evenly on the p-GaN along the lateral channel direction. However, this gate architecture leads to high electric eld (E- eld) at the p-GaN edge near p-GaN/AlGaN junction, resulting in immature hard breakdown in the gate stack upon a small $V_{GS}$. A percolation path may be formed in the AlGaN barrier after gate breakdown [21], [22], shorting the p-GaN and 2-D electron gas channel through which the drain terminal is connected. Consequently, the p-GaN/AlGaN/GaN junction (p-i-n diode) which is the key to block high OFF-state $V_{DS}$ (reverse biased p-i-n diode) under normal circumstances is destroyed, resulting in signi cant increase of reverse $I_G$.

In this work, for the rst time, we have demonstrated a high-voltage p-GaN HEMT with OFF-state blocking capability after forward gate breakdown, by properly managing the E- eld distribution in the gate stack thus keeping the p-GaN/AlGaN/GaN junction intact. Although the forward $I_G$ increased signi cantly after forward gate breakdown, preventing the device from further normal operation, the OFF-state drain voltage and reverse gate leakage blocking capability are preserved in the device. We demonstrate such capability in our p-GaN HEMTs that exhibit a high $V_{BR}$ of 1100 V at $I_D$ of 1 $\mu$A/mm with grounded substrate, a low $R_{ON}$ of 1.8 m$\Omega \cdot$cm$^2$, and a maximum $I_D$ ($I_{DS,max}$) of 610 mA/mm, which are comparable to state-of-the-art device results.

## II. Device Design and Fabrication

The MOCVD grown p-GaN/AlGaN/GaN heterostructure on a 6-inch Si substrate is from a commercial supplier. The epitaxial structure consists of a 5-$\mu$m high-resistivity GaN buffer, a 400-nm i-GaN channel, a 10-nm $Al_{0.2}Ga_{0.8}N$ barrier, and a 70-nm Mg-doped p-GaN cap, as shown in Fig. 1. The hole concentration in the p-GaN layer after

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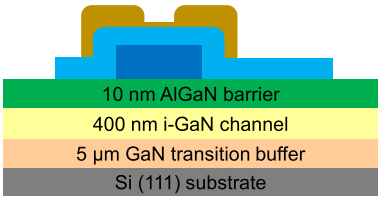
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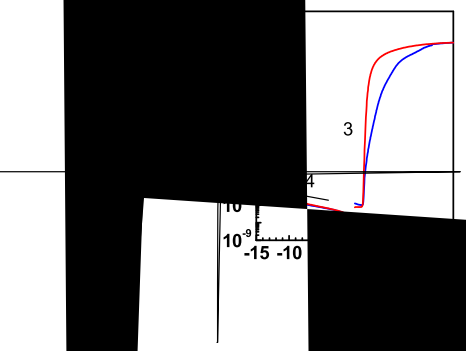
400 nm i-GaN channel
5 µm GaN transition buffer
Si (111) substrate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